

HD74HCT1G04

Inverter

REJ03D0193-0500Z
(Previous ADE-205-303C (Z))
Rev.5.00
Jan.28.2004

Description

The HD74HCT1G04 is high-speed CMOS inverter using silicon gate CMOS process. With CMOS low power dissipation, it provides high-speed equivalent to LS-TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output.

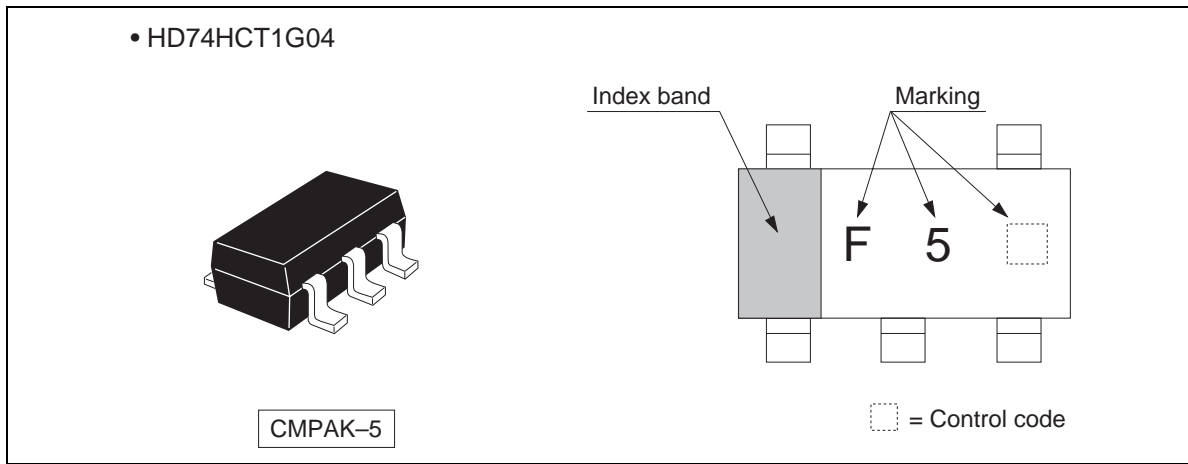
Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.
Supply voltage range : 4.5 to 5.5 V
Operating temperature range : -40 to +85°C
- $|I_{OH}| = I_{OL} = 2 \text{ mA (min)}$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT1G04CME	CMPAK-5 pin	CMPAK-5V	CM	E (3,000 pcs/reel)

HD74HCT1G04

Outline and Article Indication



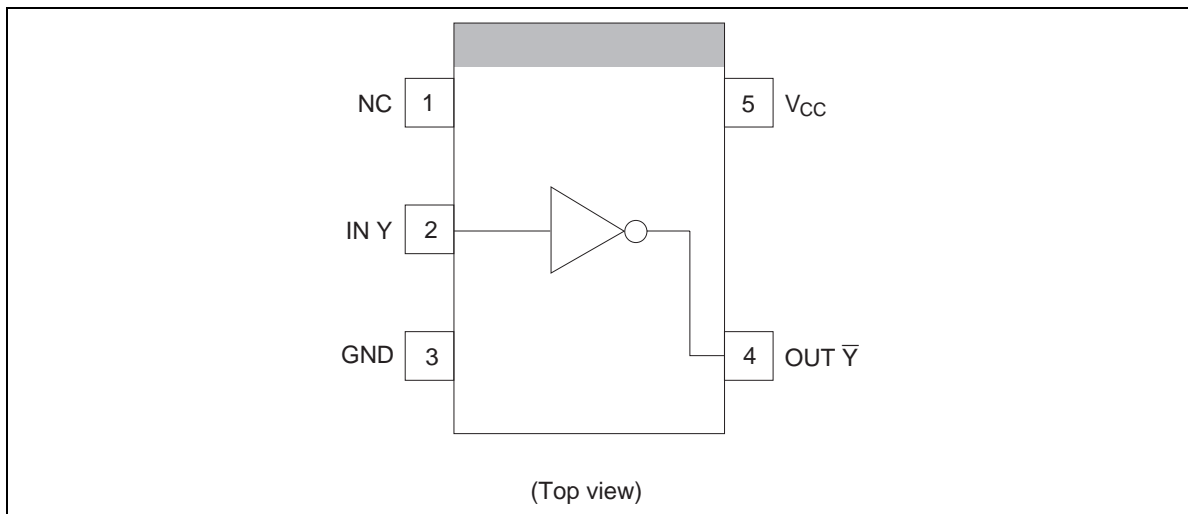
Function Table

Input A	Output \bar{Y}
H	L
L	H

H : High level

L : Low level

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to $V_{CC} + 0.5$	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	Output : H or L
Input clamp current	I_{IK}	±20	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±20	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±25	mA	
Maximum power dissipation P_T at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}		200	mW	
Storage temperature	T_{stg}	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Test Conditions
Supply voltage range	V_{CC}	4.5	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OL}	—	2	mA	$V_{CC} = 4.5$ to 5.5 V
	I_{OH}	—	-2		$V_{CC} = 4.5$ to 5.5 V
Input rise / fall time (0.3 V to 2.7 V)	t_r, t_f	0	500	ns	$V_{CC} = 4.5$ to 5.5 V
Operating temperature	T_a	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristics

Item	Symbol (V)	V _{CC}	T _a = 25°C			T _a = -40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V _{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V	
	V _{IL}	4.5 to 5.5	—	—	0.8	—	0.8		
Output voltage	V _{OH}	4.5	4.4	4.5	—	4.4	—	V	V _{IN} = V _{IL} I _{OH} = -20 μA
		4.5	4.18	4.31	—	4.13	—		I _{OH} = -2 mA
	V _{OL}	4.5	—	0.0	0.1	—	0.1		V _{IN} = V _{IH} I _{OL} = 20 μA
		4.5	—	0.17	0.26	—	0.33		I _{OL} = 2 mA
Input current	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND
Operating current	I _{CC}	5.5	—	—	1.0	—	10.0	μA	V _{IN} = V _{CC} or GND
Quiescent supply current	I _{CCCT}	5.5	—	—	2.0	—	2.9	mA	One input V _{IN} = 2.4 V, other input V _{CC} or GND

Switching Characteristics

Item	Symbol	Ta = 25°C			Unit	Test Conditions
		Min	Typ	Max		
Output rise / fall time	t _{TLH}	—	6	10	ns	Test circuit
	t _{THL}					
Propagation delay time	t _{PLH}	—	7.5	12	ns	Test circuit
	t _{PHL}	—	10	17		

(C_L = 15 pF, t_r = t_f = 6 ns, V_{CC} = 5 V)

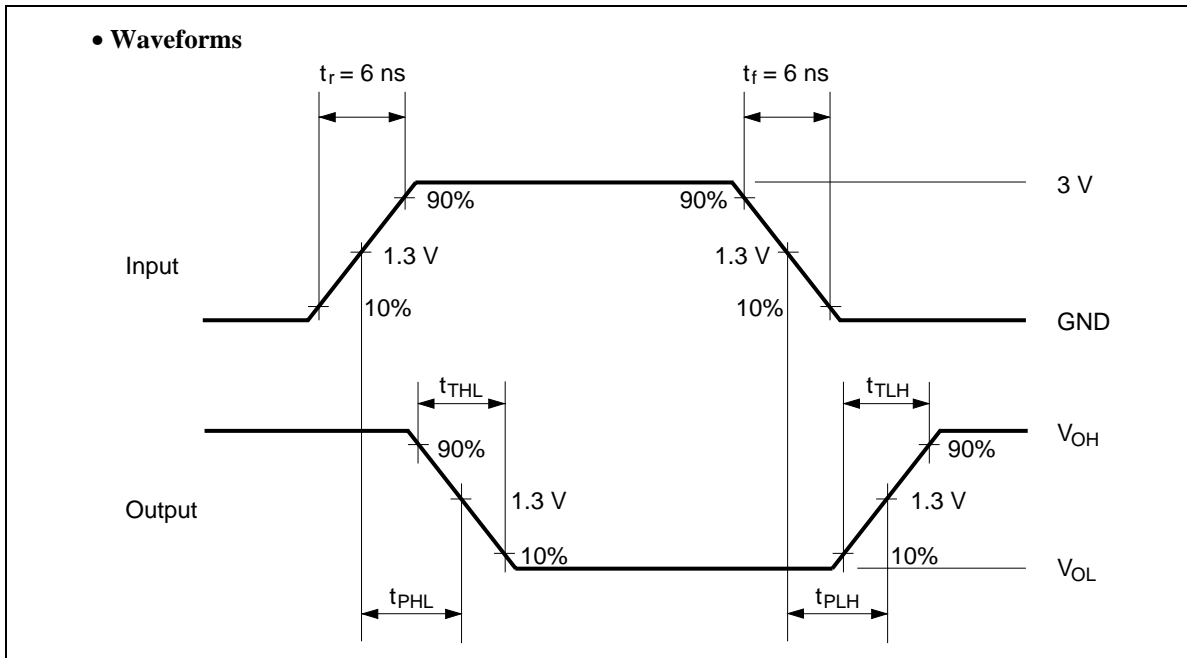
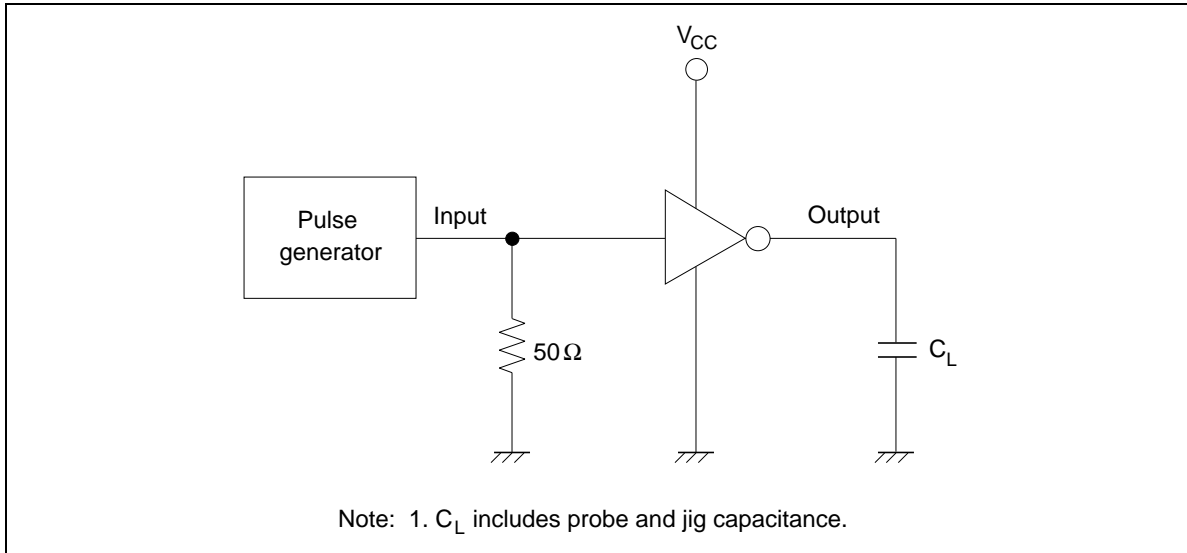
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Output rise / fall time	t _{TLH}	4.5	—	14	25	—	31	ns	Test circuit
	t _{THL}								
Propagation delay time	t _{PLH}	4.5	—	11.2	16	—	20	ns	Test circuit
	t _{PHL}	4.5	—	16.4	27	—	31		
Input capacitance	C _{IN}	—	—	2.5	5	—	5	pF	
Equivalent capacitance	C _{PD}	—	—	10	—	—	—	pF	

(C_L = 50 pF, t_r = t_f = 6 ns)

Note: C_{PD} is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

$$I_{CC} (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Test Circuit



Package Dimensions



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